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SECTION 1

INTRODUCTION

1.1 DESCRIPTION

CTF 40052 VIDEO DISPLAY CONTROLLER (VDC) IS A TAL-004 LOW POWER SCHOTTKY GATE ARRAY USED FOR PROVIDING MONOCHROME DISPLAY USING NTSC VIDEO MONITOR, A HOME TELEVISION SET CAN BE USED WHEN THE OUTPUT OF THE VDC IS MODULATED USING AN EXTERNAL MODULATOR. THE VDC GENERATES ALLL NECESSARY VIDEO, CONTROL AND SYNCHRONIZATION SIGNALS. THE DISPLAY INFORMATION IS STORED IN EXTERNAL MEMORY WHICH IS SHARED BETWEEN THE VDC AND THE CPU. THE CPU PLACES THE REQUIRED DISPLAY AND CONTROL INFORMATION IN THE MEMORY WHICH IS RETRIEVED BY THE VDC TO GENERATE THE COMPOSITE VIDEO.

THE VDC HAS TWO VIDEO DISPLAY MODES: STANDARD, AND BIT MAP. THE STANDARD MODE PROVIDES 24 ROWS OF 32 CHARACHTERS EACH. EACH CHARACTER IS 8X8 PIXELS . THERE CAN BE UP TO 128 UNIQUE CHARACTERS IN EACH SCAN OF THE DISPLAY. THE DIFINITION OF THESE CHARACTERS IS EXPECTED IN THE ASSIGNED MEMORY LOCATIONS. THE BIT MAP MODE PROVIDES 256 X 192 PIXELS DISPLAY. THE DISPLAY INFORMATION IS EXPECTED TO BE IN THE RELEVENT MEMORY AREA.

THE VIDEO OUTPUT IS EITHER BLACK OR WHITE WITHOUT ANY SHADES OF GRAY. THE BORDER AND DISPLAY CAN BE SELECTED BLACK OR WHITE INDEPENDENT OF EACH OTHER.

1.2 FEATURES

* SINGLE CHIP MONOCHROME VIDEO CONTROLLER
* 256 X 192 DISPLAY RESOLUTION
* STANDARD (CHARACTER) AND BIT MAP MODES OF OPERATION
* NTSC COMPOSITE VIDEO OUT
* STANDARD 40 PIN PACKAGE

1.3 TYPICAL APPLICATIONS

* VIDEO TERMINALS
* HOME COMPUTERS
* A TYPICAL SYSTEM IMPLEMENTATION USING THE VIDEO DISPLAY CONTROLLER IS SHOWN IN FIG. 1-1.

1.4 DEFINITIONS

* PIXEL - THE SMALLEST POINT ON THE TV SCREEN THAT CAN BE INDEPENDENTLY CONTROLLED.
* NTSC - NATIONAL TELEVISION STANDARDS COMMITTEE WHICH SPECIFIES THE TELEVISION SIGNAL STANDARD FOR THE USA.
* COMPOSITE VIDEO - COMBINED SYNC, BLANKING AND VIDEO SIGNAL.

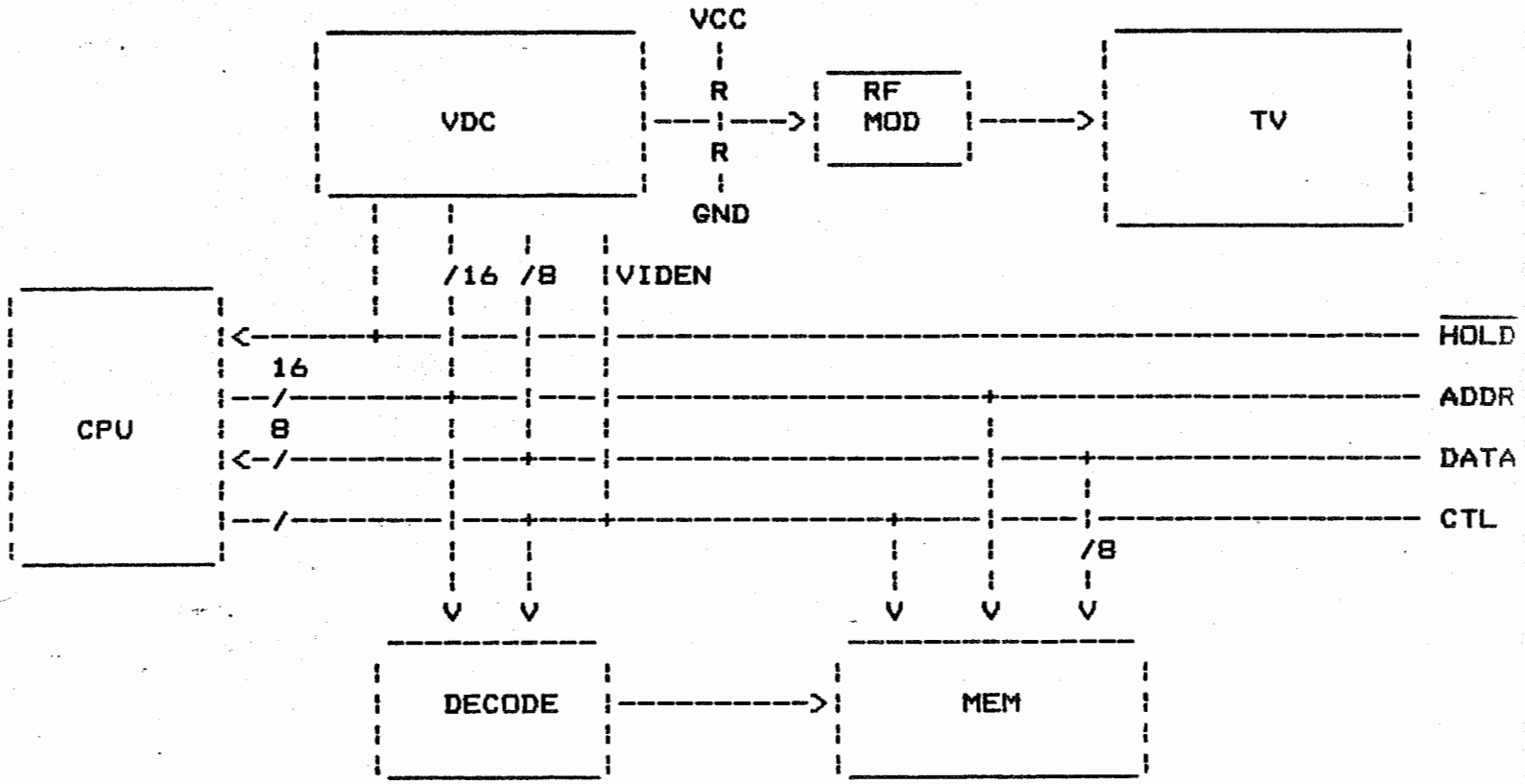


FIGURE: 1-1 SYSTEM BLOCK DIAGRAM

SECTION 2

ARCHITECTURE

2.0 ARCHITECTURE

THE VIDEO DISPLAY CONTROLLER IS DESIGNED TO PROVIDE A SIMPLE INTERFACE BETWEEN A MICROPROCESSOR AND A RASTER SCANNED TELEVISION SET. FIG. 2-1 IS A BLOCK DIAGRAM OF THE MAJOR PORTIONS OF THE VDC ARCHITECTURE. DESCRIBED BELOW ARE DETAILS OF VARIOUS INTERFACES TO THE CPU, MEMORY AND TELEVISION SET.

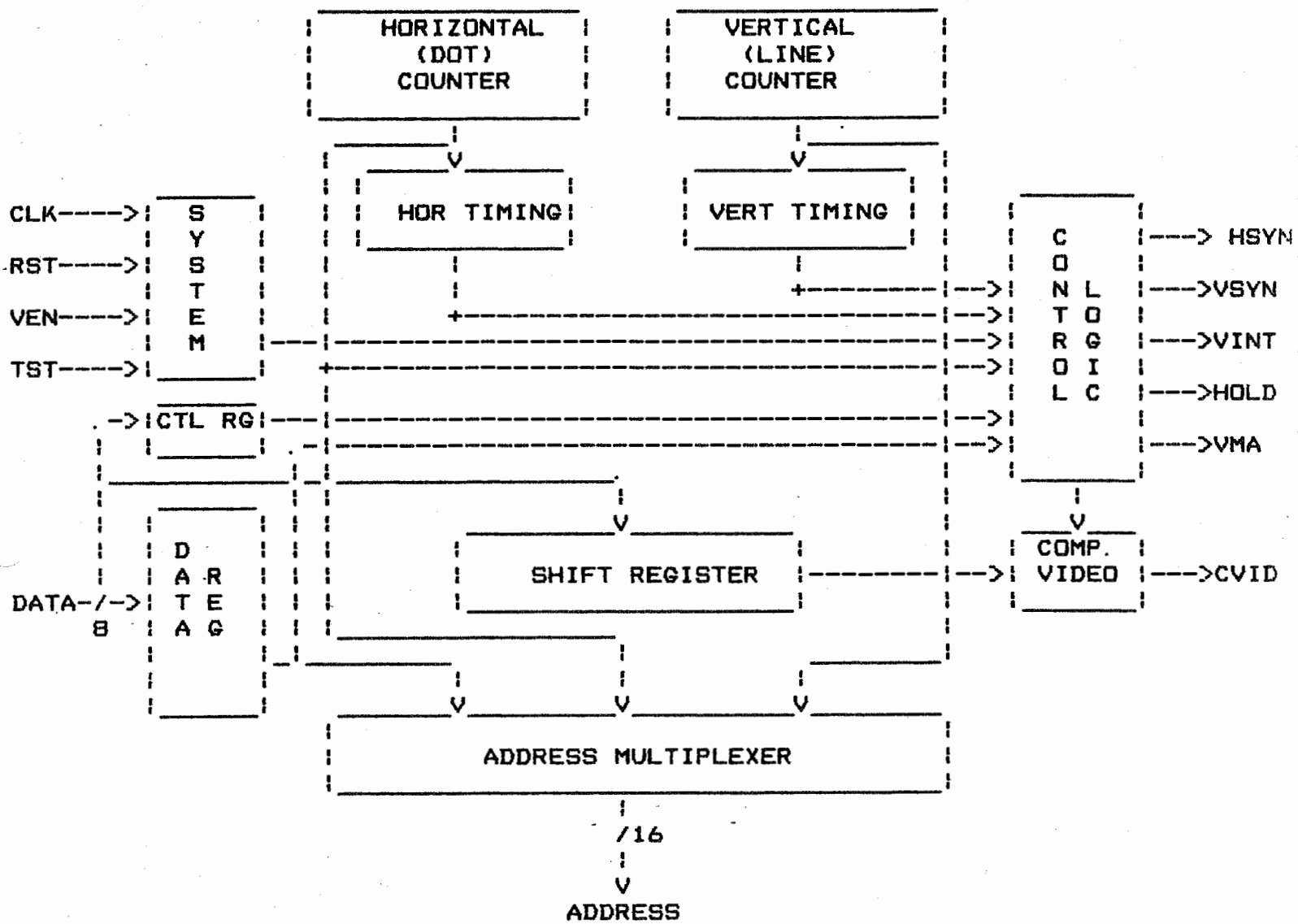


FIGURE: 2-1 CTF 40052 VDC BLOCK DIAGRAM

2.1 CPU INTERFACE

THE VDC OPERATES AS A DMA DEVICE. THE CPU CAN INHIBIT THE VDC FROM ACCESSING THE MEMORY OR ISSUING A HOLD TO THE CPU BY ASSERTING VIDEN HI. IF THE HOLD IS ACTIVE BEFORE VIDEN GOES HI THE VDC REMOVES HOLD AND PUTS THE ADDRESS BUS IN HI IMPEDENCE IN (CLOCKS/NSEC) OF VIDEN GOING HI. WHILE VIDEN IS LO THE VDC KEEPS THE SCREEN WHITE.

2.2 MEMORY INTERFACE

THE VDC CAN ONLY READ FROM THE EXTERNAL MEMORY. THE INFORMATION RETRIEVED FROM THE MEMORY IS EITHER DISPLAY OR CONTROL INFORMATION. THE VDC PROVIDES A COMPLETE 16 BIT ADDRESS FOR THE MEMORY LOCATION THAT NEEDS TO BE ACCESSED. CHIP SELECT DECODES ARE DONE EXTERNAL TO THE VDC.

2.3 TELEVISION INTERFACE

THE VDC HAS A COMPOSITE VIDEO OUT PIN. THIS SIGNAL IS LOW FOR SYNC, HI Z FOR BLACK AND HI FOR WHITE. A RESISTOR DIVIDER IS NEEDED EXTERNALLY TO PROVIDE THE REQUIRED LEVEL FOR BLACK. THE COMPOSITE VIDEO CONTAINS ALL THE NECESSARY SYNC, BLANKING AND VIDEO INFORMATION AND CAN BE FED DIRECTLY TO A VIDEO MONITOR. FOR USING A TELEVISION SET AN RF MODULATOR WOULD BE REQUIRED.

2.4 CONTROL REGISTER

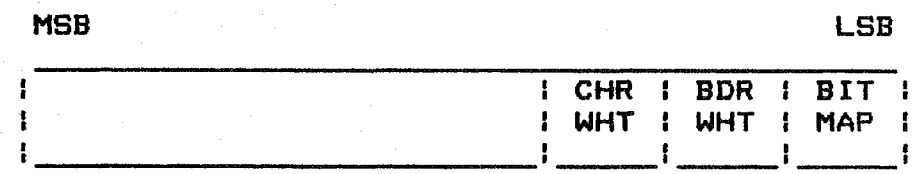
THE VDC HAS A THREE BIT CONTROL REGISTER ON BOARD. IF THE VIDEN IS LO , THIS REGISTER IS UPDATED FROM THE MEMORY LOCATION 6F00 (HEX) ONCE EVERY 1/60 SEC.. ONLY THE LEAST SIGNIFICANT THREE BITS ARE LOADED IN THE CONTROL REGISTER . THE CPU UPDATES THE RAM LOCATION FOR PROPER CONTROL OF THE VDC OPERATION. BIT ASSIGNMENTS FOR THE RAM WORD AND THE CONTROL REGISTER ARE SHOWN IN FIG. 2.4.1

ON RESET THE CONTROL BITS ARE SET AS SHOWN BELOW

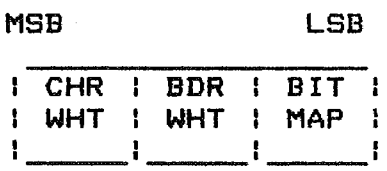
BIT MAP=LO

BORDER WHITE=HI

CHARACTER WHITE=HI



BIT ASSIGNMENT FOR RAM LOCATION 6F00 (HEX)



BIT ASSIGNMENT FOR VDC CONTROL REGISTER

FIGURE: 3-4-1 VDC CONTROL PARAMETERS

2.5 BASIC TIMING

DISPLAY ON A TELEVISION SCREEN IS CREATED BY SCANNING A LINE AT A TIME. EACH LINE IS COMPOSED OF A NUMBER OF DOTS. THE VDC USES A 9 BIT HORIZONTAL AND A 9 BIT VERTICAL COUNTER TO PROVIDE ALL THE NECESSARY TIMING INFORMATION FOR GENERATING COMPOSITE VIDEO AND CONTROL SIGNALS.

HORIZONTAL COUNTER KEEPS THE COUNT OF THE DOT BEING SCANNED ON A LINE WHILE THE VERTICAL COUNTER KEEPS THE COUNT OF THE LINE. HORIZONTAL COUNTER INCREMENTS EVERY CYCLE OF THE CLOCK. ON REACHING A COUNT OF 341 IT RESETS TO ZERO AND THE VERTICAL COUNTER IS INCREMENTED BY 1. AFTER THE VERTICAL COUNTER HAS COUNTED UPTO 261 IT RESETS TO ZERO.

FIGURE 2.5.1 SHOWS THE CORRESPONDENCE OF THE COUNTERS TO THE SCREEN TIMING

HORIZONTAL COUNTER

COUNT	# OF DOTS/CLOCKS	SCREEN TIMING
0-255	256	DISPLAY AREA
256-270	15	RIGHT BORDER
271-278	8	RIGHT BLANKING
279-304	26	HOR. SYNC
305-328	24	LEFT BLANKING
329-341	13	LEFT BORDER
	TOTAL=342	

VERTICAL COUNTER

VERT. COUNT	# OF LINES	SCREEN TIMING
0-191	192	DISPLAY AREA
192-217	26	BOTTOM BORDER
218-220	3	BOTTOM BLANKING
221-223	3	VERT. SYNC
224-236	13	TOP BLANKING
237-261	25	TOP BORDER
	TOTAL=262	

FIGURE: 2-5-1 VDC COUNTERS AND SCREEN TIMING

2.6 STANDARD MODE

IN STANDARD MODE THE DISPLAY ON THE SCREEN IS COMPRISED OF 24 ROWS OF 32 CHARACTERS. EACH CHARACTER IS COMPOSED OF 8X8 PIXELS. THESE CHARACTERS ARE SEQUENTIALLY ADDRESSED FROM 0-767. THE FIRST CHARACTER OF THE FIRST FIRST ROW HAS THE ADDRESS 0 AND THE LAST OF THE LAST ROW HAS ADDRESS 767.

AN ADDRESS TABLE OF 768 BYTES WITH 1 BYTE FOR EACH CHARACTER LOCATION ON SCREEN EXISTS IN THE EXTERNAL MEMORY STARTING FROM MEMORY ADDRESS EC00 (HEX). A BYTE RETREIVED FROM THIS TABLE ADDRESSES THE DESCRIPTION TABLE HOLDING 128 - 8X8 BIT DESCRIPTION BLOCKS. THE DESCRIPTION TABLE STARTS FROM MEMORY ADDRESS 1C00 (HEX)

THE VDC ACCESSES BOTH THE ADDRESS TABLE AND THE DESCRIPTION TABLE TO PRODUCE THE REQUIRED CHARACTERS ON THE SCREEN A LINE AT A TIME. ANY TIME THE CONTENTS OF THE RETREIVED BYTE FROM THE ADDRESS TABLE ARE OVER 127 IT IS INTERPRETED AS AN END OF LINE INDICATION AND THE VDC WOULD RELEASE HOLD FROM THAT TIME TILL THE NEXT LINE CYCLE IS INITIATED.

FIGURE 2.6.1 GRAPHICALLY SHOWS THE SEQUENCE OF EVENTS AND THE CORRESPONDENCE OF THE SCREEN, ADDRESS TABLE AND THE DESCRIPTION TABLE.

FIGURE 2.6.2 SHOWS THE SYSTEM TIMING FOR THE STANDARD MODE OPERATION AND FIGURE 4.4 EXPLAINS THE TIMING PARAMETERS.

THE VDC CAN PROVIDE 32 CHARACTERS/LINE, BUT SOME TELEVISIONS MAY NOT BE ABLE TO SHOW ALL OF THESE BECAUSE OF OVERSCAN. IN ORDER NOT TO LOOSE INFORMATION IT IS RECOMMENDED THAT THE FIRST AND THE LAST TWO CHARACTERS NOT BE USED.

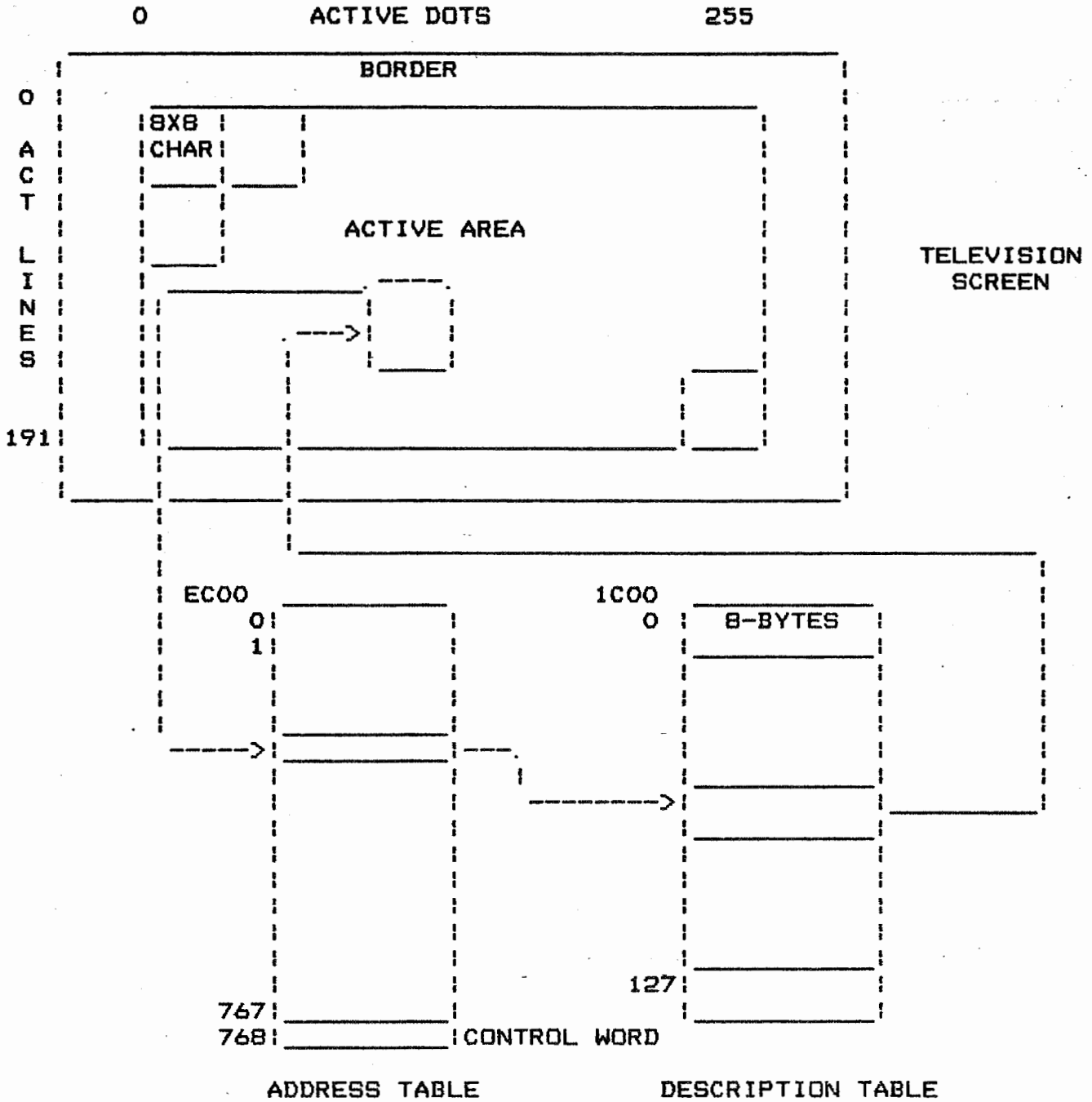
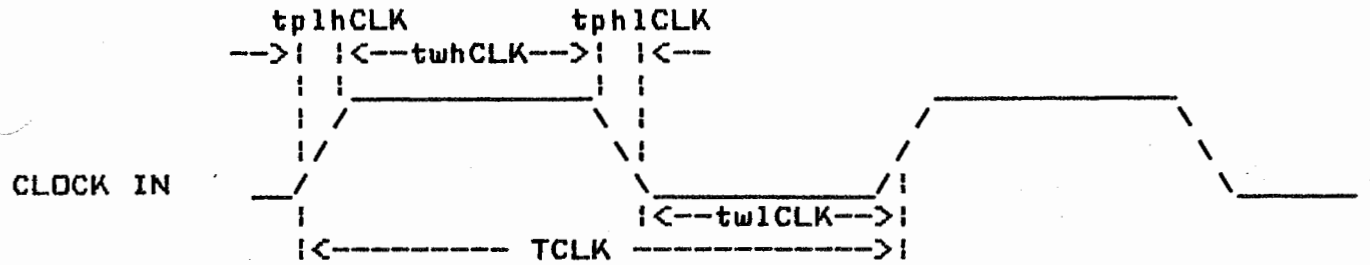


FIGURE: 2-6-1 STANDARD MODE OPERATION


tplhCLK
tphlCLK
twhCLK
CLOCK IN
twlCLK
TCLK

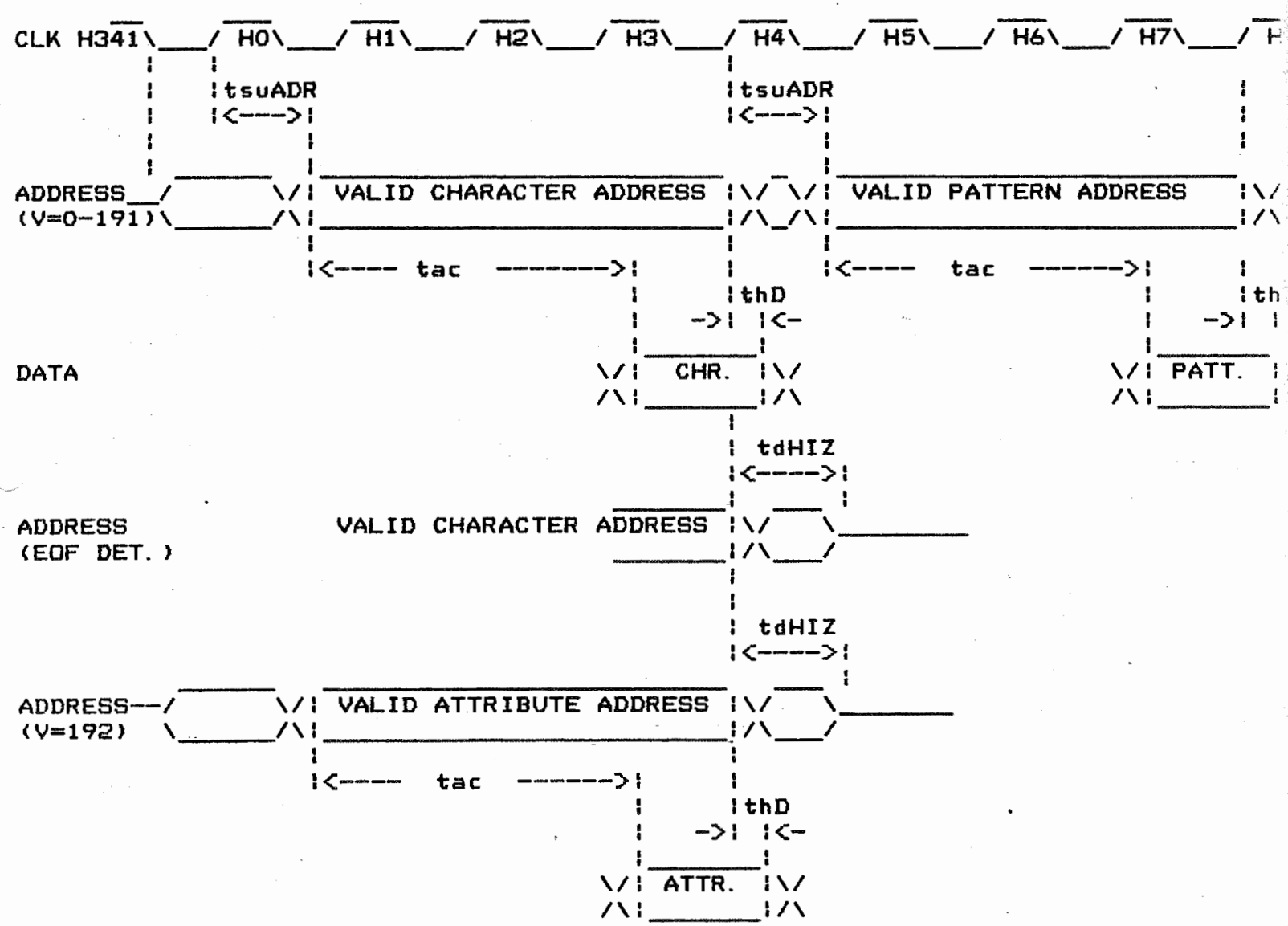

CLK H341
H0
H1
H2
H3
H4
H5
H6
H7
tsuADR
ADDRESS
(V=0-191)
VALID CHARACTER ADDRESS
VALID PATTERN ADDRESS
tac
thD
DATA
CHR.
PATT.
tdHIZ
ADDRESS
(EOF DET.)
ADDRESS
(V=192)
VALID ATTRIBUTE ADDRESS
ATTR.

FIGURE: 2-6-2 STANDARD MODE SYSTEM TIMING

2.7 BIT MAP MODE

THE INFORMATION TO BE DISPLAYED IS PLACED IN A 6K BYTE RESERVED AREA IN THE MEMORY STARTING AT ADDRESS E000 (HEX). THE VDC RETREIVES THE FIRST BYTE FROM THIS AREA AND GENERATES THE FIRST EIGHT PIXELS ON THE FIRST LINE. THE SECOND BYTE GENERATES THE NEXT EIGHT PIXELS AND SO ON.

FIGURE 2.7.1 SHOWS THE SEQUENCE OF THE DISPLAY GENERATION IN THE BIT MAP MODE.

FIGURE 2.7.2 SHOWS THE SYSTEM TIMING FOR BIT MAP MODE OPERATION AND FIGURE 4.4 EXPLAINS THE TIMING PARAMETERS.

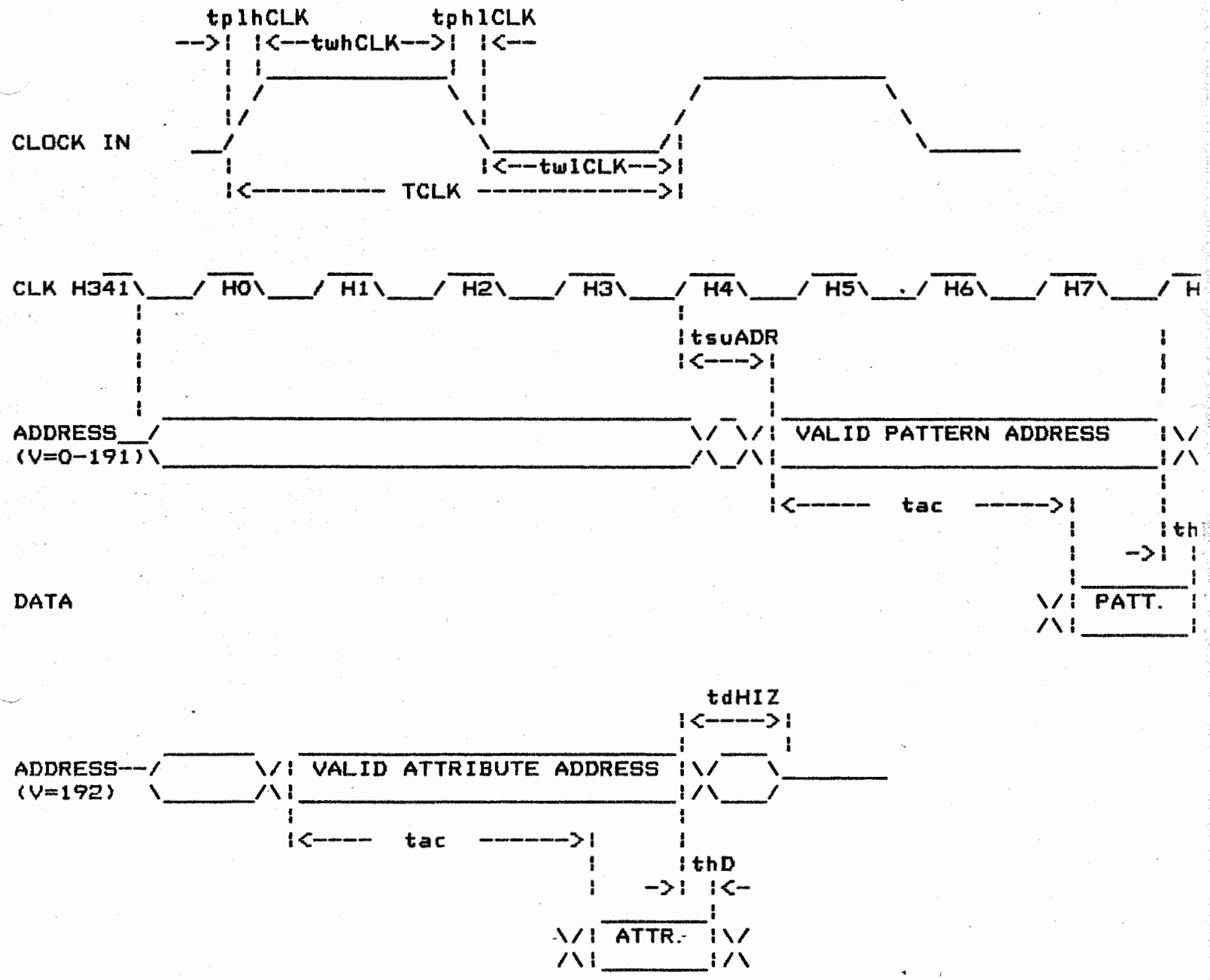


FIGURE: 2-7-2 BIT MAP MODE SYSTEM TIMING

SECTION 3

VDC PIN ASSIGNMENTS

SIGNATURE	PIN#	I/O	DESCRIPTION
A0	9	OUT	ADDRESS OUT
A1	8	"	" "
A2	7	"	" "
A3	6	"	" "
A4	5	"	" "
A5	4	"	" "
A6	3	"	" "
A7	2	"	" "
A8	1	"	" "
A9	39	"	" "
A10	38	"	" "
A11	37	"	" "
A12	36	"	" "
A13	35	"	" "
A14	34	"	" "
A15	33	"	" "
D0	30	IN	DATA IN
D1	29	"	" "
D2	28	"	" "
D3	27	"	" "
D4	26	"	" "
D5	25	"	" "
D6	24	"	" "
D7	23	"	" "
GND	10	IN	POWER
VIDEN*	11	IN	VIDEO ENABLE
HOLD*	12	OUT	HOLD CPU
COMPVID	13	OUT	COMPOSITE VIDEO
HSYNC*	14	OUT	HORIZONTAL SYNC
VSYNC*	15	OUT	VERTICAL SYNC
OPEN	16	-	NOT USED
OPEN	17	-	NOT USED
VINT*	18	OUT	VERTICAL INTERRUPT
TST*	19	IN	TEST PIN
CLK	20	IN	CLOCK
VCC	21	IN	POWER
RST*	22	IN	RESET
GND	31	IN	POWER
VMA*	32	OUT	VALID MEMORY ACCESS
VCC	40	IN	POWER

SECTION 4

ELECTRICAL SPECIFICATION

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE AIR TEMPERATURE RANGE

Supply Voltage, Vcc	7 V
Input Voltages	7 V
Continuous Power Dissipation	
Operating Free-Air Temperature	0C TO 70C
Storage Temperature	-65C TO 150C

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VCC Supply Voltage	4.75	5.0	5.75	V
IOH High Level Output Current			-400	uA
IOL Low Level Input Current			8	mA
Ta Operating Free Air Temp	0		70	C

4.3 OPERATING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ICC Supply Current	outputs open				mA
VOH High Level Output Voltage	IOH =-400uA VCC = 4.75V	2.7	3.35		V
VOL Low Level Output Voltage	IOL = 8.0mA VCC = 4.75V		0.35	0.5	V
IOS Short Circuit Output Current	VCC = 5.25V	-20	-60	-100	mA
IOZH Off State Output Current High Level Voltage Applied	VCC = 5.25V VO = 2.7 V			20	uA
IOZL Off State Output Current Low Level Voltage Applied	VCC = 5.25V VO = 0.4 V			-20	uA
VIH High Level Input Voltage		2.0			V
VIL Low level Input Voltage				0.8	V
VIK Input Clamp Voltage	IK = -18mA			-1.5	V
IIH High Level Input Current	Vcc = 5.25V VI = 2.7 V			40	uA
IIL Low Level Input Current	Vcc = 5.25V VI = 0.4 V			-200	uA
II Input Current	Vcc = 5.25V VI = 7.0 V			100	uA
Ci Input Capacitance				15	pF

4.4 TIMING REQUIREMENTS

PARAMETER		MIN.	TYP.	MAX.	UNITS
TCLK	CLOCK CYCLE TIME		186		NS
tplhCLK	CLOCK RISE TIME				NS
tphlCLK	CLOCK FALL TIME				NS
twhCLK	CLOCK HIGH TIME				NS
twlCLK	CLOCK LOW TIME				NS
tsuADR	ADDRESS SET UP TIME				NS
thD	DATA HOLD TIME				NS
tdHIZ	ADDRESS BUS TO HI Z DELAY				NS
tac	MEMORY ACCESS TIME	500			NS